Lead-free Green

6V / 500mA Low Drop-out Linear Regulator

Description

JLR9193 is a high-performance low drop-out linear regulator with input voltage range at 2 ~ 6V and output current up to 500mA. The drop-out voltage is very low at 210mV over output at 3.3V / 300mA. Despite of the already low quiescent current at 36μA, the current consumed by the device can go further down to 0.01μA once the device is "disabled". However, the device can resume quickly to full operation within 25μs from the rising edge of the enable signal.

Noise performance of the device is exceptional with PSRR = 75dB @ 1kHz. Output noise is as little as 45μV_{RMS}. Coupled with outstanding line regulation at 0.03%, the device is a perfect fit to battery-operated wireless IoT terminals at the edge of access network. Operation integrity is further fortified with full suite of protection features (thermal shut-down, short-circuit handling, current limiting). The device delivers accurate (± 2%) output voltage at fixed levels: 1.8V, 2.8V, 3.3V.

JLR9193 is manufactured [halogen, lead, antimony] free and RoHS compliant. Packages offered are: DFN1010-4L, SOT-23-5L.

Applications

- Voltage regulation for loads sensitive to EMI hazards, and in systems where low on-demand power consumption is essential
- Mainboards in networked and battery-operated IoT Terminals
- Peripheral Board or Wireless Module inside Connected Devices, Wearables, Mobile Systems, Edge Terminals in Access Network

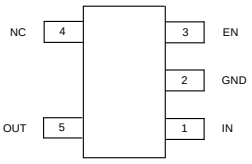
Features and Benefits

- Wide input voltage range at 2 ~ 6V and load current up to 500mA
- Drop-out voltage as low as 210mV given output at 3.3V / 300mA
- Low quiescent current at 36μA and shut-down current down to 0.01μA
- High accuracy (tolerance of V_{OUT} = ± 2%) voltage output
- Exceptional PSRR performance of 75dB at 1kHz
- Outstanding line regulation of 0.03% at I_{LOAD} = 200mA and load regulation of 0.2% at I_{LOAD} = 1 ~ 300mA
- Stable operation with MLCC capacitors (1.0μF / 1.0μF) of X6S & X7R types close to input & output pins over wide range of T_A from -40ºC to 85ºC
- Fault protection for over-current, short-circuit, over-temperature
- Lead-free packages assembled with 'green' molding compound

Pin Assignment

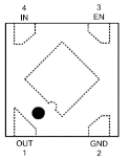
SOT-23-5L

(Top View)



DFN1010-4L

(Top View)



Ordering Information

JLR9193 X XX

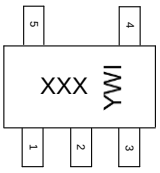
Product Prefix	Package	Output Voltage
	S5: SOT-23-5L DAP: DFN1010-4L	18: V_{OUT} = 1.8V 28: V_{OUT} = 2.8V 33: V_{OUT} = 3.3V

Product Name	Package	Marking	MSL	T_A (ºC)	Media	Quantity (pcs)
JLR9193DAP-18	DFN1010-4L	J318	3	-40 ~ 85	7" T&R	10,000
JLR9193DAP-28		J328				
JLR9193DAP-33		J333				
JLR9193S5-18	SOT-23-5L	J318	3	-40 ~ 85	7" T&R	3,000
JLR9193S5-28		J328				
JLR9193S5-33		J333				

Marking Information

SOT-23-5L

(Top View)

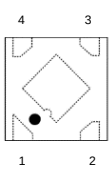


First Line: Marking (see *Ordering Information*)

Second Line: Date Code
Y: Year of Molding
W: Work-week of Molding
I: Internal Code

DFN1010-4L

(Top View)



Typical Application Circuit

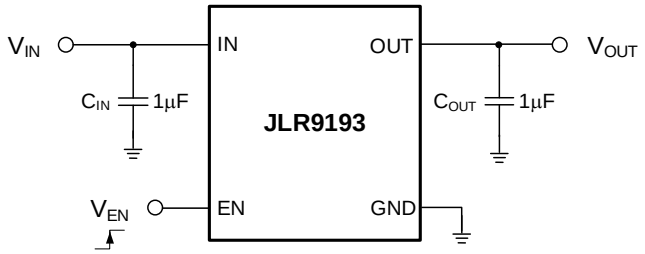


Fig. 1: Application Circuit

Functional Blocks

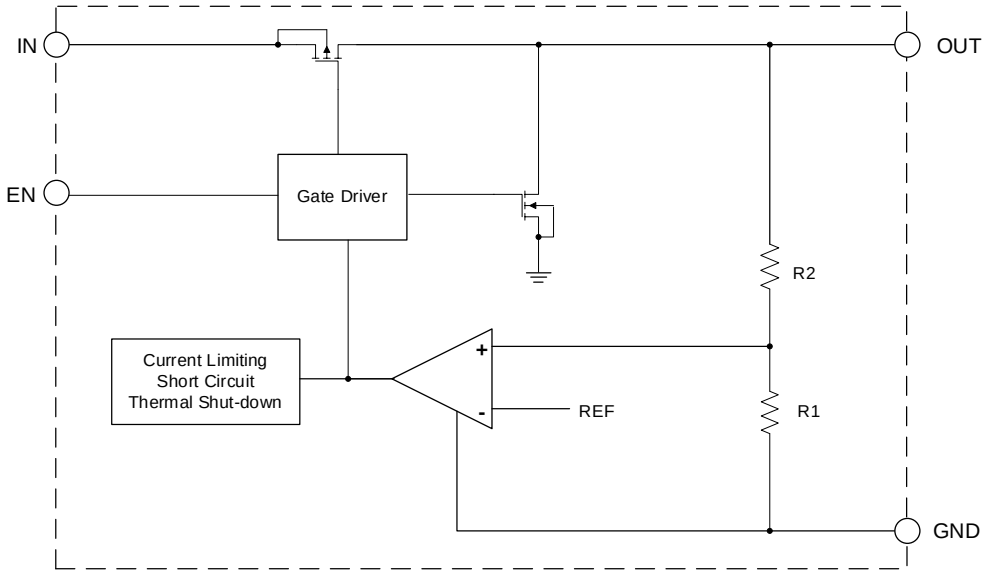


Fig. 2: Diagram of Internal Functional Blocks

Absolute Maximum Ratings *1

Symbol	Parameter	Conditions	Rating	Unit
V_{IN}	Input Voltage at IN-pin	-	-0.3 ~ 6.5	V
T_J	Operating Junction Temperature	-	150	ºC
T_{STG}	Storage Temperature Range	-	150	ºC
T_L	Lead Temperature	Soldering, 10s	300	ºC
HBM	ESD (Human Body Model)	-	4	kV
CDM	ESD (Charged Device Model)	-	0.2	kV

Notes 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. While these are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” are not implied. Exposure to “Absolute Maximum Ratings” over extended periods may adversely affect the device reliability.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IN}	Input Voltage at IN-pin	IN to GND	2.0	6.0	V
I_{OUT}	Output Current	-	-	0.5	A
V_{EN}	Input Voltage at EN-pin	EN to GND	-	V_{IN} + 0.3	V
T_A	Operating Ambient Temperature	-	-40	85	ºC

Electrical Characteristics

Test Conditions {V_{IN} = V_{EN} = [V_{SET} + 1.0V] where V_{SET} = V_{OUT} @ 1.8 / 2.8 / 3.3V; I_{OUT} = 1mA; C_{IN} = 1.0µF (ceramic); C_{OUT} = 1.0µF (ceramic); T_A = 25°C] are applicable to the following measurements unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating Input Voltage	-	2.0	-	6.0	V
V_{OUT}	Output Voltage	I_{OUT} = 1mA; -40ºC ≤ T_A ≤ 85ºC	V_{SET} * 0.98	V_{SET}	V_{SET} * 1.02	V
I_{LIMIT}	Current Limit		-	500	-	mA
I_Q	Quiescent Current	V_{EN} = V_{IN}	-	50	-	µA
I_{SHDN}	Quiescent Current at Device-OFF	V_{EN} = 0V	-	0.01	1.00	µA
V_{DROP}	Drop-out Voltage	I_{OUT} = 300mA; V_{SET} = 1.8V	-	380	520	mV
		I_{OUT} = 300mA; V_{SET} = 2.8V	-	250	400	
		I_{OUT} = 300mA; V_{SET} = 3.3V	-	210	360	
Reg_{Load}	Load Regulation, ΔV_{OUT} / V_{OUT}	1mA ≤ I_{OUT} ≤ 300mA	-	0.2	0.7	%
Reg_{Line}	Line Regulation, ΔV_{OUT} / V_{OUT}	I_{OUT} = 10mA; [V_{SET} + 1V] ≤ V_{IN} ≤ 5.5V	-	0.03	0.20	%
V_N	Output Noise Voltage	I_{OUT} = 200mA; V_{OUT} = 1.8V 10 ~ 100kHz; C_{OUT} = 1µF	-	50	-	μV_{RMS}
		I_{OUT} = 200mA; V_{OUT} = 2.8V 10 ~ 100kHz; C_{OUT} = 1µF	-	70	-	
PSRR	Power Supply Rejection Ratio	I_{OUT} = 20mA; C_{OUT} = 1µF; f = 1kHz	-	75	-	dB
		I_{OUT} = 30mA; C_{OUT} = 1µF; f = 10kHz	-	65	-	
t_{ON}	Start Time	from [V_{EN} = V_{IN}] to [90% of V_{SET}]	-	25	-	µs
V_{ENH}	EN Input Voltage for Logic 'H'	Device turned ON	1.5	-	-	V
V_{ENL}	EN Input Voltage for Logic 'L'	Device turned OFF	-	-	0.3	V
R_{EN-PD}	Pull-down Resistance at EN-pin		0.8	1	1.3	MΩ
T_{TSD}	Thermal Shut-down Threshold		-	155	-	°C
$T_{TSD-Hys}$	Thermal Shut-down Hysteresis		-	20	-	°C

Thermal Properties

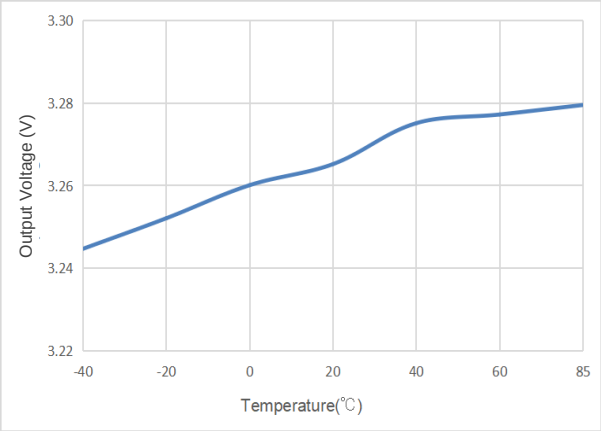
Test Conditions: Device mounted on FR-4 substrate, 2-layer PCB, 2oz copper, with minimum recommended cooling pad to dissipate heat

Symbol	Parameter	Package	Rating	Unit
$R_{\Theta JA}$	Thermal Resistance (junction-to-ambient)	SOT-23-5L	200	ºC/W
		DFN1010-4L	300	

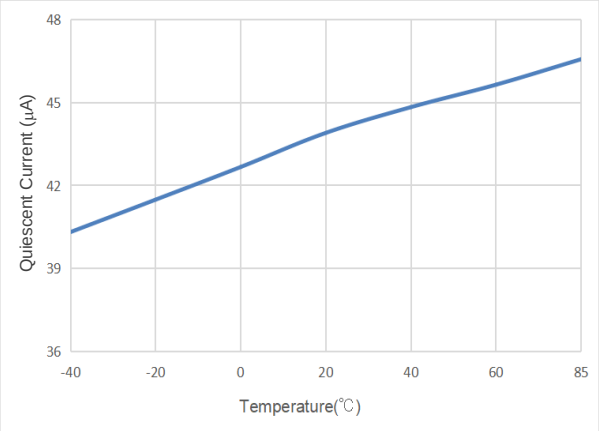
Performance Characteristics

Test Conditions [V_{IN} = 4.3V; I_{OUT} = 1mA; C_{IN} = 1.0µF (ceramic); C_{OUT} = 1.0µF (ceramic); T_A = 25°C] are applicable to the following measurements unless otherwise stated.

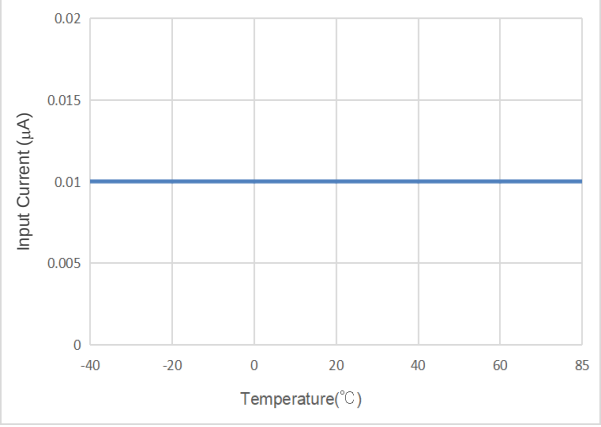
Graph 1: Output Voltage vs. Temperature



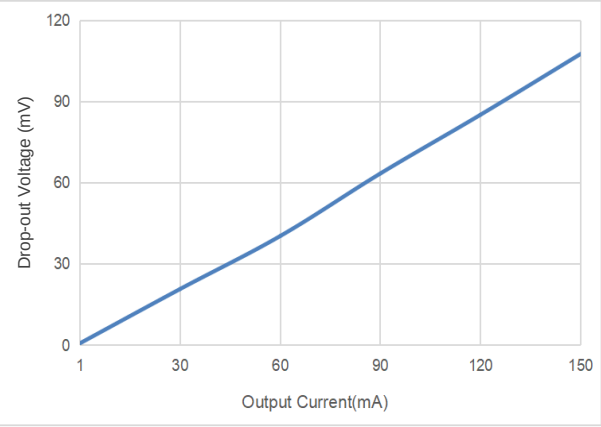
Graph 2: Quiescent Current vs. Temperature



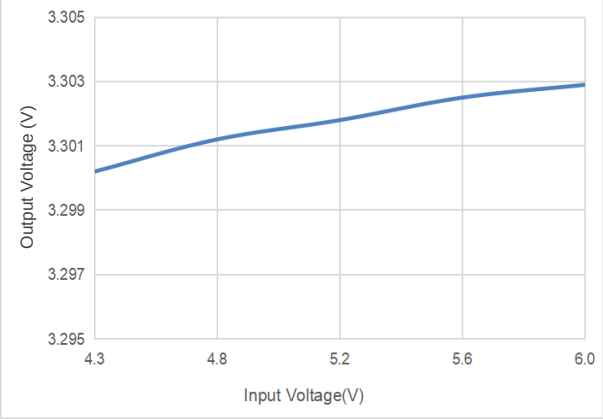
Graph 3: Input Current During Shut-down vs. Temperature



Graph 4: Drop-out Voltage vs. Output Current



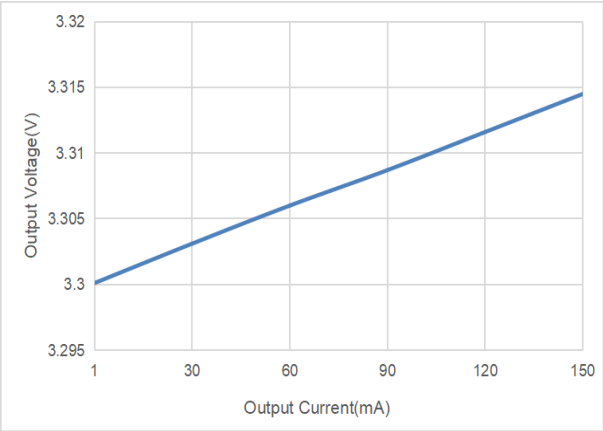
Graph 5: Output Voltage vs. Input Voltage



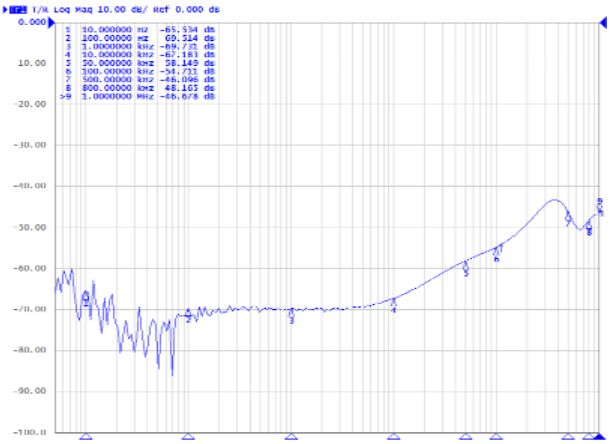
Performance Characteristics (Continued)

Test Conditions [V_{IN} = 4.3V; I_{OUT} = 1mA; C_{IN} = 1.0µF (ceramic); C_{OUT} = 1.0µF (ceramic); T_A = 25°C] are applicable to the following measurements unless otherwise stated

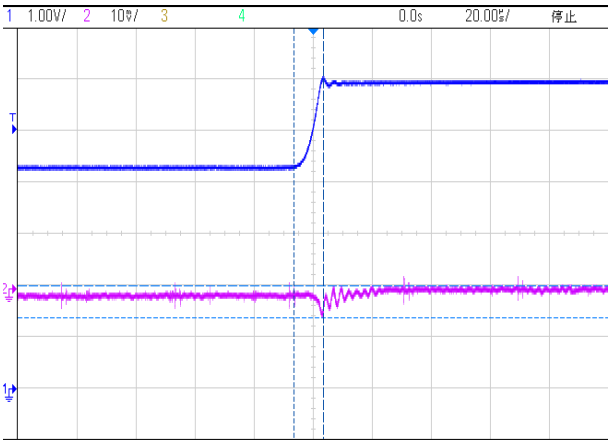
Graph 6: Output Voltage vs. Output Current



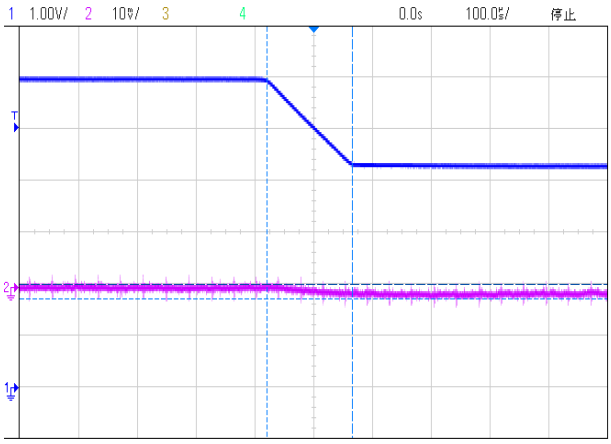
Graph 7: PSRR vs. Frequency



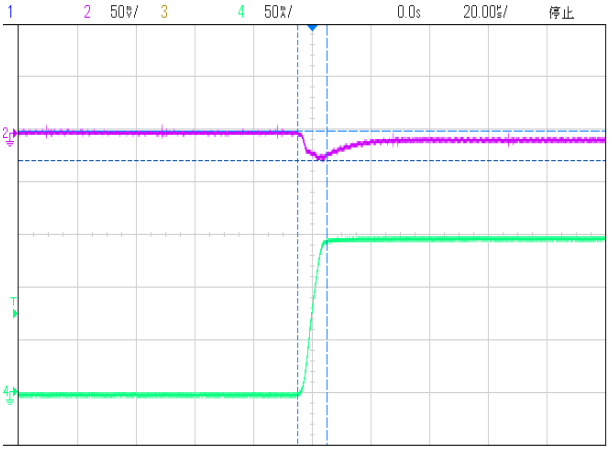
Graph 8: Line Transient (V_{IN} = 4.3V ➔ 6V; I_{OUT} = 10mA; t = 10µs)



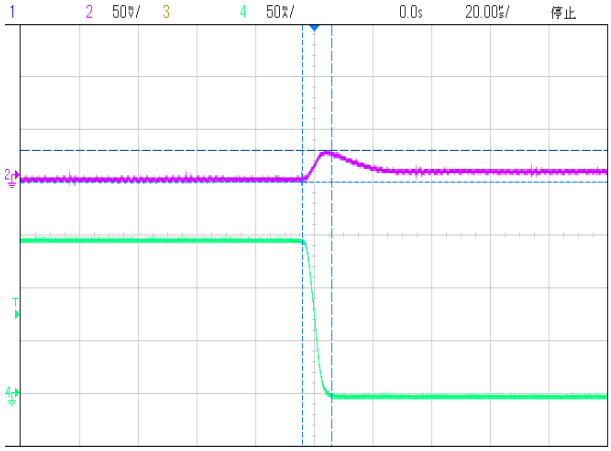
Graph 9: Line Transient (V_{IN} = 6V ➔ 4.3V; I_{OUT} = 10mA; t = 10µs)



Graph 10: Load Transient (I_{OUT} = 1mA ➔ 150mA; t = 10µs)



Graph 11: Load Transient (I_{OUT} = 150mA ➔ 1mA; t = 10µs)



Detailed Description of Device Operation

Overview

The JLR9193 is a high-performance linear regulator with input voltage up to 6.0V, and fixed output voltage levels (1.8V, 2.8V, 3.3V) at up to 500mA. While it operates on quiescent current as little as 36μA, the PSRR performance stands at the exceptional 75dB over 10Hz ~ 100kHz, output voltage noise is as low as 45μV_{RMS} at I_{OUT} = 200mA over the same frequency range. Should ultra-long battery time be required, the device can be disabled to keep the current consumption to as low as 0.01μA. Response to transients occurred at the line input and the output load are swift at 0.03% and 0.2% accordingly.

Input & Output

In order to de-couple the noise and glitch present on the power line at the input of JLR9193 and the circuit board on which the device is adopted, input capacitor (C_{IN}) of ceramic type with value of 1μF as close as possible to the IN pin is recommended. Value of the C_{IN} shall fall within the range 0.47 ~ 4.70μF. Wide copper trace is required between the IN and the GND pins.

Output capacitor (C_{OUT}) of ceramic type with value of 1μF is recommended to be placed as close as possible to the OUT pin. While higher capacitance could potentially improve the load & line regulation performance and have the over-shoots and under-shoots minimized, care must be taken to ensure that the equivalent ESR do not adversely affect the high-frequency noise immunity as well as unexpected shift in phase response hence output stability. Values of the ESR and the C_{OUT} shall fall within the range 5 ~ 100mΩ and within the range 0.47 ~ 4.70μF respectively.

In order to minimize the temperature dependence of the application circuit, either X6S or X7R type is recommended for both the input and output capacitors.

Enable Feature

The device can be turned ON or OFF by driving the EN pin to either logic 'H' or logic 'L'. To ensure proper operation of the device, this pin must not be left unconnected. If the enable function is not used, this pin must be tied to the IN pin at all time such that the device remains at ON state all the time.

Current Protection

When the current appearing at the OUT pin goes up higher than the current limit designated for the device, or when the OUT & GND pins are shorted together, the built-in over-current and short-circuit protection shall be triggered. Upon the occurrence of such hazard, the output current (I_{OUT}) shall be limited by the internal logics to approximately 500mA. As a result, the device is protected from damage due to over-heat.

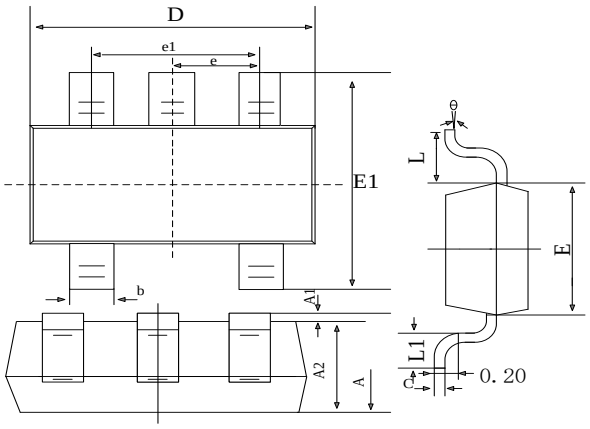
Thermal Protection & Power Dissipation

When the junction temperature (T_J) of the silicon die assembled inside the device goes up beyond the normality at close to 155ºC, due either to excessive loading or short-circuit at the OUT pin, the built-in thermal shut-down protection shall be triggered. The on-die power MOSFET shall be turned OFF to prevent the device from electrical overload. At this time, the device shall operate on hiccup mode under which the output shall be enabled momentarily every so often. Should the over-temperature phenomenon persists due to the combination of power dissipation of the device, thermal resistance of the package, ambient temperature and the expiration of any circuit hazard, hiccup mode shall continue.

As soon as the abnormality disappears such that the junction temperature of the die comes down to approximately 130ºC, the device shall resume its typical operation and drive the load connected to the OUT pin normally.

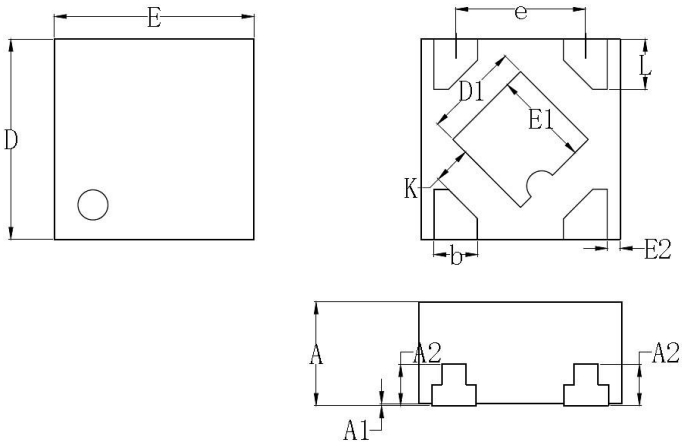
Package Outline (All measurements in mm)

Package Type: SOT-23-5L (J1)



SOT-23-5L (J1)		
Dimension	Min.	Max.
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.85	3.05
E	1.50	1.70
E1	2.65	2.95
e	0.95 (BSC)	
e1	1.80	2.00
L	0.30	0.60
θ	0°	8°
All measurements in "mm"		

Package Type: DFN1010-4L (J1)



DFN1010-4L (J1)			
Dimension	Min.	Typ.	Max.
A	0.45	0.50	0.55
	0.50	0.55	0.60
A1	0.00	-	0.05
A2	0.203 TIY		
b	0.17	0.22	0.27
D	0.95	1.00	1.05
D1	0.43	0.48	0.53
E	0.95	1.00	1.05
E1	0.43	0.48	0.53
E2	0.065 TIY		
e	0.650 BSC		
K	0.200 BSC		
L	0.20	0.25	0.30
All measurements in "mm"			

Disclaimer

The information presented in this document are for reference only. Yangzhou Yangjie Electronic Technology Co., Ltd. (a.k.a. YJ) reserves the right to make changes without prior notice to the specification of the product displayed herein to improve reliability, function, design or otherwise.

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